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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,560	11/17/2003	Simon Charles Watt	550-479	6835

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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,560	WATT ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. **10/714,560** has a total of *15* claims pending in the application; there are *2* independent claims and *13* dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. 201.14(c),** acknowledgement is made of applicant's claim for priority based on an application filed on November 18, 2002 (Foreign Priority 0226882.9).

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by **M.P.E.P.** 609(c), the applicant's submission of the Information Disclosure Statements dated **09/16/2004** and **11/17/2003** are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P.** 609(c), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3 and10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3 and 10 recite the limitation "said plurality of exception vector" in line 3 of claims 3 and 10. There is insufficient antecedent basis for this limitation in the claim. **[The applicant might consider amending claims 1 and 8 (previous independent claims upon which 3 and 10 are dependent) to reference the plurality of exception vectors]**.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by **Gardner et al. (U.S. PG PUB No. 2003/0101322 hereafter referred to as Gardner).**

With respect to independent **claims 1, 8 and 15**,

> *"Apparatus for processing data, said apparatus comprising: a processor* **[Gardner discloses in paragraph [0002], "Computer systems include at least one processor and memory." See FIG. 3]** *operable in a plurality of modes* **[Gardner discloses in paragraph [0189], "secure and non-secure"]** *and a plurality of domains, said plurality of domains comprising a secure domain or a non-secure domain* **["secure and non-secure user processes" Gardner also discloses in paragraph [0026], "Secure platform 40, however, ensures that one domain cannot accidentally or intentionally access another domain's memory."]***,"*

"...said plurality of modes including: at least one secure mode being a mode in said secure domain; and at least one non-secure mode being a mode in said non-secure domain; **[paragraph [0189]]***"*

*"...wherein when said processor is executing a program in a secure mode said program has access to secure data which is not accessible when said processor is operating in a non-secure mode***[Gardner discloses in paragraph [0026], "Secure platform 40, however, ensures that one domain cannot accidentally or intentionally access another domain's memory."];***"**

"...said processor includes a non-secure translation table base address register **(FIG. 3, elements 94, 96)** [Gardner discloses in **paragraph [0043], "registers that can be included in system register set 96 include ...a translation look-aside buffer"]** *operable in said non-secure domain to indicate a region of memory storing non-secure domain memory mapping data defining how virtual addresses are translated to physical addresses within said non-secure domain; and said processor includes a secure translation table base address register operable in said secure domain to indicate a region of memory storing secure domain memory mapping data defining how virtual addresses are translated to physical addresses within said secure domain***[Gardner discloses in paragraph [0047], "TLB 128 holds recently used virtual to physical memory address mappings to memory 74].***"**

With respect to **claims 2 and 9**,

"Apparatus as claimed in claim 1 **[see rejection of claim 1]**, *wherein non-secure domain memory mapping data is non-secure domain memory page table data and secure domain memory mapping data is secure domain memory page table data* **[Gardner discloses in paragraph [0189], "...the information for distinguishing between secure and non-secure user processes is contained in a secure memory page in memory 74 that cannot be modified by PL2 code." Gardner teaches that there is a memory for secure and a non-secure data Gardner further discloses in paragraph [0047], "...page table 140, which is stored in memory 74 and contains entries that each map a single memory page of memory 74." Gardner also teaches that the non-secure domain memory mapping data is non-secure domain memory page table data and secure domain memory mapping data is secure domain memory page table data]." (Also see rejection of claim 1 supra).**

With respect to **claims 3 and 10**,

"Apparatus as claimed in claim 1 **[see rejection of claim 1]**, *wherein said processor is also operable in a monitor mode* **[Gardner discloses in paragraph [0143] "area"]** *and any switching* **["handles"]** *between a secure mode and a non-secure mode* **["SPK 36"]** *said plurality of exception vector is performed via said monitor mode.* **[The switching or forming of secure/non-secure domains must go through or be performed by areas (anchors and backing paragraph [0141]). Note: the examiner interprets the instant claim sans the limitation "exception vector" for reasons stated supra.]"**

With respect to **claims 4 and 11**,

> *"Apparatus as claimed in claim 3***[see rejection of claim 3]**, *wherein when in said monitor mode* **[Gardner discloses in paragraph [0143], "area"]** *said processor does not use virtual memory addressing* **["no physical pages are associated with the virtual address range"]**."

With respect to **claims 5 and 12**,

> *"Apparatus as claimed in claim 1, wherein said non-secure translation table* **[see rejection of claim 1 above]** *base address register and said secure translation table base address register* **[Gardner discloses in paragraph [0195], "information in memory"]** *are not writable* **["memory partitions and processes to protect"]** *when said processor is in said non-secure domain* **["from all other applications and operating systems"]**." (See also **paragraph [0026]**)

With respect to **claims 6 and 13**,

> *"Apparatus as claimed in claim 1***[see rejection of claim 1]**, *wherein said non-secure translation table base address register and said secure translation table base address register exception control register are part of a configuration controlling coprocessor couple to said processor* **[As examined in the**

applicant's specification in paragraph [0102], Gardner teaches non-secure translation table base address register and said secure translation table base address register [FIG. 3, elements 94, 96, and 128] exception control register are part of a configuration controlling coprocessor [Control Registers element 124] couple to said processor [Processor element 32].]."
(See FIG. 3 elements 124, 94, 96, 128, and 32 and rejection of claim 5 supra)

With respect to **claims 7 and 14**,

"Apparatus as claimed in claim 1 **[see rejection of claim 1]**, *wherein said processor is responsive to an exception condition to select an exception handler in dependence upon an exception vector value associated with said exception condition and stored within an active exception vector table for said exception condition, said active exception vector table being one of a plurality of exception vector tables and different exception vector tables being selected for use by virtue of being mapped into a predetermined region of virtual memory by a currently active one of said non-secure domain memory mapping data and said secure domain memory mapping data* **[Gardner discloses in paragraphs [0066] and [0068]: Gardner teaches said processor [Note: the examiner notes that computer processing execution is dependent upon processor/CPU command/responses] is responsive to an exception condition [when an exception occurs] to select an exception handler [exception handler] in dependence upon an exception vector value [Table**

II] associated with said exception condition and stored within an active exception vector table for said exception condition [The exception handler assures that the stack and the RSE save area are in appropriately secured memory]. Gardner also teaches active exception vector table being one of a plurality of exception vector tables [some of the system state] and different exception vector tables being selected for use by virtue of being mapped into a predetermined region of virtual memory by a currently active one of said non-secure domain memory mapping data and said secure domain memory mapping data [TLB] (See rejection of claim 1)]."

With respect to **claim 15**,

"A computer program product having a computer program operable to control a data processing apparatus in accordance with a method as claimed in claim 8."

[Gardner disclosed in paragraph [0008], "An operating system image is stored in the memory for controlling the processor and the memory, and operates on top of the secure platform."]

CONCLUSION

Status of Claims in the Application

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i):**

Claims rejected in the Application

Per the instant office action, claims **1-15** have received a first action on the merits and are subject of a first action non-final.

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more

information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

Horace L. Flournoy

Patent Examiner

Art unit: 2189

Supervisory Patent Examiner

Technology Center 2100